IN THE CLAIMS:

Claim 1 - 4 (canceled)

5. (Currently Amended) An electronic phase-locked loop for the jitter-attenuated generation of an output clock signal which is phase-synchronous with respect to a reference clock signal, the phased lock loop comprising ~~a circuit having~~:

a digitally controllable oscillator with,

a drive circuit connected to said digitally controllable oscillator for digitally setting the output clock signal of the digitally controllable oscillator so that a phase error between the output clock signal and a reference clock signal, is zero,

a digital phase detector ~~for~~ comparing the output clock signal of the oscillator with the reference clock signal,

an analog phase detector ~~in parallel with said digital phase detector~~,

a lock detection circuit connected to said digital phase detector and said analog phase detector for avoiding a phase quantization error,

~~said~~wherein the lock detection circuit ~~activating~~activates the analog phase detector to run simultaneously with said digital phase detector if the phase error is zero,

the activated analog phase detector regulating the output clock signal of the digitally controllable oscillator in a continuously variable manner until the respective clock signal edges of the output clock signal and of the reference clock signal are fully synchronous,

the lock detection circuit deactivating the analog phase detector and continuously checking and ~~activating~~regulating the digital phase detector until the phase error between the output clock signal and the reference clock signal does not exceed a specific phase error.

6. (previously presented) The electronic phase-locked loop as claimed in claim 5, further including a PI filter with an integral regulation, a linear regulation and an addition and amplifier stage, which is driven by the analog phase detector.